REMARKS

Claims 1-20 are pending in this application, of which claims 1, 11, 19 and 20 are independent. Applicant amends claims 1, 11, 19 and 20 and the specification as detailed above. For the following reasons, this application should be considered in condition for allowance and passed to issue.

The Office Action rejects claims 1-3, 7, and 19 under 35 U.S.C. §102(e) as being anticipated by Crotty (U.S. Patent NO. 6,160,431) and rejects claims 11, 16-18 and 20 under 35 U.S.C. §103(a) as being unpatentable over the same reference. Applicant acknowledges with appreciation the Examiner's indication that claims 4-6, 8-10 and 12-15 would be allowable if rewritten in independent form.

An aspect of the present invention is defined in claim 1 as including, in a semiconductor integrated circuit device, a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of the first power supply voltage to activate a first power-on detection signal according to a result of detection. A second power-on detection circuit responsive to a second power supply voltage detects power-on of the second power supply voltage to activate a second power-on detection signal according to a result of detection. A main power-on detection circuit is coupled to the first and second power-on detection circuits and generates a main power-on detection signal, which is rendered active from activation of the first activated power-on detection signal of the first and second power-on detection signals until inactivation of the second activated power-on detection signal of the first and second power-on detection signals.

Independent claims 11, 19, and 20 have been amended to include various certain of the above features and/or variations thereof.

Crotty intends to prevent malfunction of the internal logic circuit in uncertain or indefinite state of the input signal due to insufficient voltage applied to the input/output circuit, and in particular, intends to prevent the signal/data transfer between input/output circuits and the internal circuit when the first power supply voltage is at an insufficient level and the second power supply voltage is at a sufficient level. This is accomplished by a power-on reset circuit for dual-voltage logic devices, which is configured to reset an internal circuit upon a power-on condition. Particularly, the first power supply voltage Vcc1 is supplied to the input/output circuit and the second power supply voltage Vcc2 is supplied to the internal logic circuit. Dual detection circuit 210 determines whether Vcc1 is greater than a predetermined voltage. When the voltage level of the first power supply voltage Vcc1 is insufficient, the internal circuit receiving the second power supply voltage for operation is reset. Therefore, Crotty is directed to detection of a single power application sequence. Specifically, when the first power supply voltage is applied while the second power supply voltage is not applied, the power on reset signal POR is activated, as shown in Figs. 3(b), 3(d), and Fig. 8 of Crotty.

Rejection under 35 U.S.C. §102(e)

Applicants respectfully traverse the rejection of claims 1-3, 7, and 19. In rejecting the claims, Fig. 9 of Crotty is relied upon to show the power-on detection circuit of the present invention. The Office Action correlates detection circuit 210 and

dual-detection circuit 630 with the claimed first power-on detection circuit and the second power-on detection circuit, respectively. Further, the Office Action correlates the claimed main power-on detection circuit with the OR gate 950 of Fig. 9 and the first inverter 512 in the delay-line circuit 940. Applicants respectfully disagree with the Office Action's characterization and traverses the rejection.

Applicants submit that the claimed main power-on detection circuit embodied by the independent claims is fully distinguishable from and patentable over the Crotty reference. The Office Action takes the position that the main power-on detection circuit of claim 1 reads on the dual-input low pass filter 930 of Crotty. However, the dual-input low pass filter 930 fails to operate in the claimed manner. The dual-input low pass filter 930 of Fig. 9 replaces individual low pass filters, as illustrated by Fig. 6 (Col. 10, lines 35-38), and serves the purpose of removing short transient power off logic levels (Col. 9, lines 15-18), thereby increasing device integrity. By contrast, claim 1 recites "a main power-on detection circuit...rendered active from activation of first activated power-on detection signal...until inactivation of second activated power-on detection signal..." Applicants have thoroughly reviewed the reference but is unable to find any disclosure or suggestion of the low pass filter 930 or any components thereof (OR gate 950) functioning as the claimed main power-on detection circuit, and moreover, any disclosure or suggestion of the main power-on detection circuit by Crotty.

Claim 19 recites "a main power-on detection circuit...for activating a main power-up detection signal from activation of a first activated power-up detection signal

in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state." As set forth above, the low pass filter and components thereof such as the OR gate are configured to remove transient signal levels. By contrast, the recited main power-on detection circuit of claim 11 is configured to activate/inactivate a main power-up detection signal in the claimed manner, which holds an internal circuit in a reset state. The low pass filter and OR gate of Crotty fails to operate in the foregoing claimed manner.

Accordingly, claims 1 and 19 are fully distinguishable from the Crotty reference. Claims dependent therefrom are further patentable at least based on their dependency and for the reasons recited above. Applicants respectfully request that the rejection of claims 1-3, 7, and 19 under 35 U.S.C. §102(e) is reconsidered and withdrawn.

Rejection under 35 U.S.C. §103(a)

Applicants respectfully traverse the rejection of claims 11, 16-18, and 20 under 35 U.S.C. §103(a). Figure 9 is again relied upon. The Office Action correlates the claimed internal voltage application detection circuit with the dual detection circuit 210, correlates the claimed power-on detection circuit with the detection circuit 630 and correlates the claimed main detection circuit with OR gate 950. The Office Action acknowledges that Crotty does not disclose the claimed internal voltage generation circuit, but states that it would have been obvious to use a voltage step-down circuit to generate the reduced voltage. The Office Action further states that it would have been

obvious to use the step-down circuit for generating the internal voltage Vcc1..."if the design value of the internal voltage is higher than a voltage level which the circuit provides." Applicants respectfully disagree with the Office Action's characterization.

Claim 11 is patentable over the Crotty reference as Crotty fails to disclose or suggest the main power-on detection circuit, as set forth above. Claim 11 recites "a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of internal voltage power-up detection signal and the power-on detection signal." The OR gate 950 of the low pass filter 930, which removes transient signal levels, is incapable of functioning as the claimed main power-on detection circuit, as suggested and for the reasons set forth above.

Claim 20 recites "main power-on detection circuit responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state." The claimed main power-on

detection circuit is neither disclosed nor suggested by Crotty, for the same reasons. Additionally, there is no disclosure or suggestion of the low pass filter or OR gate holding an internal circuit in a reset state, as claimed.

The Office Action acknowledges that Crotty fails to disclose or suggest the internal voltage generation circuitry of the claims, but states one of ordinary skill in the art could use a step-down circuit to generate the internal voltage. However, there is no motivation found in Crotty nor disclosed or suggested by the factual evidence in the record to alter the Crotty reference in the suggested manner. It is believed that the motivation set forth by the Office Action has been based on subjective belief and unknown authority, which renders an obviousness rejection invalid.

Accordingly, for these reasons, it is believed that rejected claims 11 and 20 are patentable over the Crotty reference. Claims dependent therefrom are also patentable at least based on their dependency and for the reasons recited above. Withdrawal of this rejection is respectfully solicited.

Conclusion

While Applicants gratefully acknowledge the Examiner's indication of the allowability of certain claims, it is believed the amended independent claims now more particularly recite features distinguishing these claims from the cited reference. In view of the above amendments, it is respectfully submitted that all claims, remaining in the application are now in condition for allowance. An early notice to that affect is earnestly solicited. Applicants encourage the Examiner to contact Applicants'

undersigned representative regarding measures to progress this application to a condition for allowance.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX - MARKED-UP VERSION

IN THE SPECIFICATION:

Page 13, first full paragraph was amended as follows:

When the power supply voltage VDDL is applied or powered on at Tc, the power-on detection signal /PORL has its level once increased in response to the rising of the power supply voltage VDDL and then fixed at the "L" level. The output signal of the inverter 12b responsively attains the "H" level of the power supply voltage VDDL level to turn on the MOS transistor 12c. The node [12b] 12m is again reliably coupled to the ground node and held at the ground voltage level.

Page 13, second full paragraph was amended as follows:

When the power supply voltage VDDL is stabilized at time Td, the power-on detection signal /PORL attains the "H" level and the output signal from the inverter 12h responsively attains the "H" level of the power supply voltage [VDDH] VDDL. Responsively, the MOS transistors 12i and 12j are both turned on to discharge the node 12n to the ground voltage level, so that the main power-on detection signal /POROH from the inverter 12k attains the "H" level. Thus, when both of the power supply voltages VDDL and VDDH attain the stable state, the main power-on detection signal /POROH enters the "H" level inactive state.

Page 22, third full paragraph was amended as follows:

The bit line precharge/equalization control circuit 22, the bit line isolation control circuit 23, the sense amplifier control circuit 24, the main word line drive circuit 20 and the sub-decoder 21 have the same structures as those of the level conversion circuit illustrated in Fig. 6 and each receives the high voltage VPP, or the DRAM power supply voltage VDDH or the array power supply voltage VDDS according to the amplitude of its output signal. To the main word line drive circuit 20, the sub-decoder 21, the bit line precharge/equalization control circuit 22, the bit line isolation control circuit 23 and the sense amplifier control circuit 24, the main power-on detection signal [/PORR] /POROH is applied. Also the write drive circuit WDR, the main power-on detection signal /POROH is applied. Also to the write drive circuit WDR, the main power-on detection signal /POROH is applied.

Page 26, second full paragraph was amended as follows:

At time T11, the logic power supply voltage VDDL is applied to have its voltage level increased. When at time T12, the logic power supply voltage VDDL is stabilized, the main power-on detection signal [POROH] /POROH attains the "H" level and the converted voltage application detection signal /POROP responsively attains the "H" level as well (boosted voltage VPP level).

Page 31, first full paragraph was amended as follows:

Fig. 14 is a diagram schematically showing a structure of a power-on detection signal generation unit according to the third embodiment of the present invention. In

Fig. 14, the power-on detection signal generation unit includes: a power-on detection circuit 40 for detecting application of the logic power supply voltage VDDL to generate a logic power-on detection signal /PORL; a boosting circuit 42 for generating the boosted voltage VPP from the DRAM power supply voltage VDDH; a high voltage application detection circuit 44 for generating a high voltage application detection signal /PORP according to the voltage level of the boosted voltage VPP from the boosting circuit 42; and a main power-on detection circuit 46 for generating a main power-on detection signal /POROP which is rendered inactive when both of the logic power-on detection signal /PORL and the high voltage [power-on] application detection signal /PORP are inactivated.

IN THE CLAIMS:

Claims 1, 11, 19 and 20 are amended as follows:

1. (Amended) A semiconductor integrated circuit device comprising:

a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;

a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage to activate a second power-on detection signal according to a result of detection; and

a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active

[while at least one of the first and second power-on detection signals is active] from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

11. (Amended) A semiconductor integrated circuit device comprising:

an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage to activate a power-on detection signal according to a result of detection; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active [while at least one of said internal voltage power-up detection signal and said power-on detection signal is active] from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of internal voltage power-up detection signal and the power-on detection signal.

19. (Amended) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages; and

a main power-on detection circuit coupled to receive the power-up detection signals for activating a main power-up detection signal [while at least one of the power-up detection signals are active] from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state

20. (Amended) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltage differing in voltage level from each other and from said at least one power supply voltage;

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at

least one power source voltage in accordance with a voltage level of said at least one power source voltage to generate at least one power-on detection signal for the respective at least one power source voltage; and

main power-on detection circuit responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active [while at least one of said at least one internal voltage power-up detection signal and said at least one power-on detection signal is active] from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.